ＡＲ５０００Ａ　PLL Lock-up Time

１．Upper & Lower Limit within the same VCO

VCO No. Receive Fr.	VCO No. Receive Fr.	L to H	H to L
L	H		
1 10.000kHz	1 29.900MHz	40ms	17ms
2A 30.000MHz	2A 174.900MHz	28ms	20ms
2B 175.000MHz	2B 339.900MHz	25ms	18ms
3A 340.000MHz	3A 499.900MHz	20ms	18ms
3B 500.000MHz	3B 674.900MHz	20ms	18ms

２．Over a 100kHz step

VCO No. Receive Fr.	VCO No. Receive Fr.	L to H
L	H	
1 15.000MHz	1 15.100MHz	8ms
2A 102.500MHz	2A 102.600MHz	4ms
2B 257.500MHz	2B 257.600MHz	4ms
3A 420.100MHz	3A 420.200MHz	3ms
3B 587.50MHz	3B 587.600MHz	3ms

３． A center frequency of VCO

VCO No. Receive Fr.	VCO No. Receive	L to H	H to L
L	H		
1 15.000MHz	2A 102.500MHz	10ms	23ms
2A 102.500MHz	2B 257.500MHz	17ms	22ms
2B 257.500MHz	3A 420.000MHz	13ms	15ms
3A 420.000MHz	3B 587.5000MHz	13ms	15ms

４． From lower to Upper Receive frequency

VCO No. Receive Fr.	VCO No. Receive Fr.	L to H	H to L
L	H		
1 10.000kHz	3A 3000.000MHz	28ms	20ms